Electronic Version
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Claims

[c1] 1. A non-volatile memory cell, comprising:
a tunnel dielectric layer disposed on a substrate;
a barrier dielectric layer disposed over the tunnel dielectric layer;
a graded charge trapping layer disposed between the barrier dielectric layer disposed and the tunnel dielectric layer, wherein a compositional ratio of the graded charge trapping layer varies from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer;
a gate conductive layer disposed on the barrier dielectric layer;
a source region and a drain region respectively disposed in the substrate along both sides of the gate conductive layer.

[c2] 2. The non-volatile memory cell as claimed in claim 1, wherein the compositional ratio of the graded charge trapping layer gradually decreases from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded

charge trapping layer adjacent to the barrier dielectric layer.

[c3] 3. The non-volatile memory cell as claimed in claim 1, wherein the compositional ratio of the graded charge trapping layer gradually increases from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer.

[c4] 4. The non-volatile memory cell as claimed in claim 1, wherein the compositional ratio of the graded charge trapping layer first gradually increases and then gradually decreases, from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer.

[c5] 5. The non-volatile memory cell as claimed in claim 1, wherein the compositional ratio of the graded charge trapping layer first gradually decreases and then gradually increases, from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer.

[c6] 6. The non-volatile memory cell as claimed in claim 1, wherein the graded charge trapping layer is a graded silicon nitride (Si_xN_y) layer.

[c7] 7. The non-volatile memory cell as claimed in claim 6, wherein the silicon/nitrogen ratio (x/y) of the graded charge trapping layer gradually decreases from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer.

[c8] 8. The non-volatile memory cell as claimed in claim 6, wherein the silicon/nitrogen ratio (x/y) of the graded charge trapping layer gradually increases from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer.

[c9] 9. The non-volatile memory cell as claimed in claim 6, wherein the silicon/nitrogen ratio (x/y) of the graded charge trapping layer first gradually increases and then gradually decreases, from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer.

[c10] 10. The non-volatile memory cell as claimed in claim 6, wherein the silicon/nitrogen ratio (x/y) of the graded charge trapping layer first gradually decreases and then gradually increases from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer.

[c11] 11. The non-volatile memory cell as claimed in claim 1, wherein a material of the tunnel dielectric layer includes silicon oxide.

[c12] 12. The non-volatile memory cell as claimed in claim 1, wherein a material of the barrier dielectric layer includes silicon oxide.

[c13] 13. A non-volatile memory cell, comprising:
a tunnel dielectric layer disposed over a substrate;
a barrier dielectric layer disposed over the tunnel dielectric layer;
a graded charge trapping layer disposed between the barrier dielectric layer disposed and the tunnel dielectric layer, wherein the graded charge trapping layer has a graded band gap and the graded band gap comprises of a plurality of trapping levels;
a gate conductive layer disposed on the barrier dielectric

layer;

a source region and a drain region respectively disposed in the substrate along both sides of the gate conductive layer.

[c14] 14. The non-volatile memory cell as claimed in claim 13, wherein the graded band gap of the graded charge trapping layer gradually decreases from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer.

[c15] 15. The non-volatile memory cell as claimed in claim 13, wherein the graded band gap of the graded charge trapping layer gradually increases from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer.

[c16] 16. The non-volatile memory cell as claimed in claim 13, wherein the graded band gap of the graded charge trapping layer first gradually increases and then gradually decreases, from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adja-

cent to the barrier dielectric layer.

[c17] 17. The non-volatile memory cell as claimed in claim 13, wherein the graded band gap of the graded charge trapping layer first gradually decreases and then gradually increases, from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer.

[c18] 18. The non-volatile memory cell as claimed in claim 13, wherein numbers of the trapping levels vary from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer, and for different positions in the graded charge trapping layer, the position with less numbers of the trapping levels has a higher potential barrier.

[c19] 19. The non-volatile memory cell as claimed in claim 13, wherein numbers of the trapping levels of the graded charge trapping layer gradually increases from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer, and the one side of the graded charge trapping layer adjacent to the tunnel dielectric layer has

a higher potential barrier.

[c20] 20. The non-volatile memory cell as claimed in claim 13, wherein numbers of the trapping levels of the graded charge trapping layer gradually decreases from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer, and the another side of the graded charge trapping layer adjacent to the barrier dielectric layer has a higher potential barrier.

[c21] 21. The non-volatile memory cell as claimed in claim 13, wherein numbers of the trapping levels of the graded charge trapping layer first gradually increases and then gradually decreases, from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer, and the both sides of the graded charge trapping layer have higher potential barriers.

[c22] 22. The non-volatile memory cell as claimed in claim 13, wherein numbers of the trapping levels of the graded charge trapping layer first gradually decreases and then gradually increases, from one side of the graded charge trapping layer adjacent to the tunnel dielectric layer to

another opposite side of the graded charge trapping layer adjacent to the barrier dielectric layer, and a middle portion of the graded charge trapping layer has a higher potential barrier.

[c23] 23. The non-volatile memory cell as claimed in claim 13, wherein a material of the tunnel dielectric layer includes silicon oxide.

[c24] 24. The non-volatile memory cell as claimed in claim 13, wherein a material of the barrier dielectric layer includes silicon oxide.

[c25] 25. The non-volatile memory cell as claimed in claim 13, wherein the graded charge trapping layer is a graded silicon nitride (Si_xN_y) layer.